WHAT WE CLAIM IS:

28. A method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material, said method including the steps of:

controlling at least one of a concentration and a distribution of defects or vacancies as a function of a process gas atmosphere; and

either producing an $Si_xO_yN_z$ oxy-nitride layer having a thickness of up to 2nm (20 angstroms) on a surface of a semiconductor, or

prior to a thermal treatment, removing a natural SiO_2 layer from a surface of a semiconductor and producing an Si_3N_4 layer having a thickness of up to 4nm (40 angstroms) on said semiconductor.

29. A method according to claim 28, wherein said defects are vacancies.

30. A method according to claim 28, wherein said defects are semiconductor substrate atoms on interstitial lattice positions.

31. A method according to claim 28, wherein a composition of the process gas is controlled.

32. A method according to claim 28, wherein a concentration of a process gas or of process gas components is controlled.

33. A method according to claim 28, wherein a partial pressure of a process gas is controlled.

34. A method according to claim 28, wherein a process gas includes a nitrogen-containing gas.

35. A method according to claim 34, wherein said process gas includes at least one of NH_3 and N_2.

36. A method according to claim 28, wherein a process gas contains no oxygen.

37. A method according to claim 28, wherein a process gas includes an oxygen-containing component.

38. A method according to claim 37, wherein said oxygen-containing component includes at least one of N_2O, NO, and H_2O.

39. A method according to claim 28, wherein a temperature behavior of a thermal treatment is controlled in terms of time.

40. A method according to claim 28, wherein said process gas atmosphere contains argon.

41. A method according to claim 35, wherein said process gas includes NH_3 having a concentration of 0 to 10,000ppm.

42. A method according to claim 41, wherein said NH_3 concentration is 2500 to 5,000ppm.

43. A method according to claim 28, wherein a thermal stressing of a semiconductor wafer is reduced to a minimum.

44. A method according to claim 28, wherein a distribution of foreign atoms within semiconductor material is controlled by means of distribution of said defects.

45. A method according to claim 44, wherein said foreign atoms include at least one of the elements of the group consisting of boron, phosphorus, As, Sb and In.

46. A method according to claim 28, wherein said method is carried out on a semiconductor doped with foreign atoms.

47. A method according to claim 28, wherein said method is carried out on a semiconductor that is to be doped.

48. A method according to claim 47, wherein said semiconductor is doped.

49. A method according to claim 28, wherein doping into said semiconductor is effected by means of at least one of gas phase doping, implantation, and diffusion by out-diffusion from a layer that is in contact with said semiconductor.